L Number	Hits	Search Text	DB	Time stamp
1	1636	438/637,640,672,675.ccls.and @ad<=19990916	USPAT; US-PGPUB	2003/03/13 14:31
2	268	(438/637,640,672,675.ccls.and @ad<=19990916) and (exposing with substrate)	USPAT; US-PGPUB	2003/03/13 14:30
5	1078	(contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))	EPO; JPO; DERWENT	2003/03/13 14:28
7	239	((contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))) and etching with (first adj (insulator or insulative or insulating or dielectric))	EPO; JPO; DERWENT	2003/03/13 14:30
8	3863	(contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))	USPAT; US-PGPUB	2003/03/13 14:29
9	679	((contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))) and (exposing with substrate)	USPAT; US-PGPUB	2003/03/13 14:29
10	284	(((contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))) and (exposing with substrate)) and (etching with (first adj (insulator or insulative or insulating or dielectric)))	USPAT; US-PGPUB	2003/03/13 14:30
11	262	((((contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))) and (exposing with substrate)) and (etching with (first adj (insulator or insulative or insulating or dielectric)))) not ((438/637,640,672,675.ccls.and @ad<=19990916) and (exposing with substrate))	USPAT; US-PGPUB	2003/03/13 14:31
13	151	(((((contact adj hole) and (second adj (insulator or insulative or insulating or dielectric))) and (exposing with substrate)) and (etching with (first adj (insulator or insulative or insulating or dielectric)))) not ((438/637,640,672,675.ccls.and @ad<=19990916) and (exposing with substrate))) and @ad<=19990916	USPAT; US-PGPUB	2003/03/13 14:32

US-PAT-NO: 5331733

DOCUMENT-IDENTIFIER: US 5331733 A

TITLE: Method for manufacturing a connection device for a semiconductor device

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A method for electrically connecting an internal wired layer through an insulating layer formed on the internal wired layer is described and comprises depositing a first conducting layer 1 on a substrate 10. An internal wired layer 1A is formed by **etching** a portion of the first conducting layer 1 utilizing a mask A. A **first insulating** layer 2 is deposited on the entire surface of the resulting structure. A second conducting layer 3 is deposited on the first insulating layer 2. An etch stop layer 3A is formed on the first insulating layer 2 and terminates on the first insulating layer and over the wired layer to define a surface of the wired layer covered by the etch stop layer and a surface of the wired layer not covered by the etch stop layer. A **second insulating** layer 4 is deposited on the entire surface of the resulting structure including on the etch stop layer 3A. A contact hole 20 is formed through the **second insulating** layer 4 and the first insulating layer 2 to expose the surface of the underlying wired layer not covered by the etch stop layer such that the etch stop covered surface of the wired layer remains covered by the overlying first insulating layer. A third conducting layer 5 for a predetermined purpose is deposited on the resulting structure including

the contact hole for electrically connecting the wired layer 1A thereto.

The connection device in a semiconductor device and a method for manufacturing the device of the present invention is defined by the claims with a specific embodiment shown in the attached drawings. For the purpose of summarizing the invention, the invention relates to a method for electrically connecting an internal wired layer through an insulating layer formed on the internal wired layer. The method comprises depositing a first conducting layer 1 on a substrate 10 and forming an internal wired layer 1A by **etching** a portion of the first conducting layer 1 utilizing a mask A. A **first insulating** layer 2 is deposited on the entire surface of the resulting structure including the internal wired layer. A second conducting layer 3 is deposited on the first insulating layer 2. An etch stop layer 3A is formed on the first insulating layer 2 and which terminates on the first insulating layer and over the wired layer to define a surface of the wired layer covered by the etch stop layer and a surface of the wired layer not covered by the etch stop layer. A **second insulating** layer 4 is deposited on the entire surface of the resulting structure including on the etch stop layer 3A. A contact hole 20 is formed through the **second insulating** layer 4 and the first insulating layer 2 to expose the surface of the underlying wired layer not covered by the etch stop layer such that the etch stop covered surface of the wired layer remains covered by the overlying first insulating layer. A third conducting layer 5 for a predetermined purpose is deposited on the resulting structure including the contact hole for electrically connecting the wired layer 1A thereto thereby

forming a connection device for a semiconductor device.

Preferably, the etch stop layer 3A is formed by **etching** the second conducting layer 3 utilizing a mask layer B and the contact hole 20 is formed by sequentially removing portions of the **second insulating** layer 4 and the **first insulating** layer 2 utilizing a contact mask C.

A further embodiment of the present invention includes a connection device for use in a semiconductor device. The connection device comprises a first conducting layer 1 deposited on a substrate 10 with an internal wired layer 1A positioned on the first conducting layer 1. A first insulating layer 2 is deposited on the entire surface of the resulting structure including the internal wired layer. An etch stop layer 3A is positioned on the first insulating layer 2 and terminates on the first insulating layer over the first conducting layer to define a surface of the first conducting layer covered by the etch stop layer and a surface of the first conducting layer uncovered by the etch stop layer. A **second insulating** layer 4 is positioned on the entire surface of the resulting structure including the etch stop layer 3A, A contact hole 20 is formed through the **second insulating** layer 4 and the first insulating layer 2 to expose only the uncovered surface of the underlying wired layer such that the covered surface of the first conducting layer remains covered by the first insulating layer. A third conducting layer 5 electrically connects the wired layer 1A through the contact hole to thereby form a connection device for a semiconductor device.

FIG. 2B represents that the **second insulating** layer 4 is deposited on the entire surface of the resulting structure including the

etch stop layer 3A. It is noted that the process step for depositing the **second insulating** layer 4 is optional and can be omitted.

FIG. 2C represents that the contact hole 20 is formed by sequentially removing portions of the **second insulating** layer 4 and first insulating layer 2 utilizing the contact mask C the arrangement of which fully described in connection with FIG. 1, so that the edge portion of the etch stop layer and the surface of the underlying wired layer 1A is exposed. Referring to the drawing, it can be appreciated that the upper width of the contact hole 20 can be obtained in the minimal line width attainable in presently used lithographic etching process, but the lower width of the contact hole 20 can be formed with a decreased width relative to the upper width thereof. Therefore, if the contact hole 20 is unintentionally misaligned during the formation process, the presence of the etch stop layer prevents the underlying substrate 10 from being exposed.

forming an internal wired layer 1A by etching a portion of the first conducting layer 1 utilizing a wired layer mask A and thereby **exposing** a portion of the **substrate** not covered by the internal wired layer 1A;

forming an internal wired layer 1A by etching a portion of the first conducting layer 1 utilizing a wired layer mask A and thereby **exposing** a portion of the **substrate** not covered by the internal wired layer 1A;

depositing a **second insulating** layer 4 on the etch stop layer and the first insulating layer;

forming a contact hole 20 through the **second insulating** layer 4 and the first

insulating layer 2 to expose the surface of the underlying wired layer not
covered by the etch stop layer such that the etch stop covered surface of the
wired layer remains covered by the overlying first insulating layer; and

depositing a third conducting layer 5 on the **second insulating** layer, and into
the contact hole formed in the **second insulating** layer 4 and the first
insulating layer 2, to electrically connect the wired layer 1A with the third
conducting layer 5, thereby forming a connection device for the semiconductor
device.

4. The method of claim 3 wherein the contact hole 20 is formed by sequentially
removing portions of the **second insulating** layer 4 and the first insulating
layer 2 utilizing a contact mask C.